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Abstract of the Disclosure

A data processor executes an instruction (JAVASW) to implement efficient interpreter functionality by combining the tasks of table jumps and thread or task switching which is controlled by a running value such as a counter or a timer. Execution of the instruction always requires a change of flow to be taken. In one form, the instruction may cause a hardware accelerator to be signaled to complete instruction execution. Additionally, a memory table containing emulation code correlated to specific byte codes may be compressed for a large number of identified byte codes by the use of separate storage. Further, use of a same portion of the memory table may occur in connection with execution of different bytecodes. While discussed in the context of Java bytecodes, the instruction is applicable to any programming language and processor architecture.